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## **Design | Semantic Scholar**

These portable electronic devices need very low power circuit design. In the low power VLSI circuits, the power dissipation is mainly caused by the charging and discharging of internal node capacitances due to the activity of transition. It is one of the main factors that will affect the dynamic power dissipation.

## **Low power VLSI circuit design - VIDHYARTI**

Low-Power Digital VLSI Design: Circuits and Systems addresses both process technologies and device modeling. Power dissipation in CMOS circuits, several practical circuit examples, and low-power techniques are discussed. Low-voltage issues for digital CMOS and BiCMOS circuits are emphasized.

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Abstract: This course will provide an in-depth discussion on the ultra-low power

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RF circuit transceiver and architecture design for Internet-of-Things (IoT) applications. By 2025, there will be up to 100 billion wireless sensor devices connected to IoT, and the cost of replacing or recharging the batteries will become one of the bottlenecks in ...

## **2021 VLSI | VLSI Circuits Short Course - 2021 VLSI**

Total Power dissipated in a CMOS circuit is sum of dynamic power, short circuit power and static or leakage power. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product.

## **Low Power VLSI Chip Design: Circuit Design Techniques**

- The objective of logic minimization is to reduce the boolean function.
- For low-power design, the signal switching activity is minimized by restructuring a logic circuit is minimized by restructuring

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a logic circuit •The power minimization is constrained by the delay, however, the area may increase.

## **Chapter 4 Low-Power VLSI Design**

head of the Ultra-Low-Power Sector at the CSEM Centre Suisse d'Electronique et de Microtechnique S.A., Neuchâtel. He is presently involved in the design and management of low-power and high-speed integrated circuits in CMOS technology. His main interests include the design of very low-power microprocessors and DSPs, low-power standard cell

## **Low-Power CMOS Circuits: Technology, Logic Design and CAD**

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Low-power VLSI circuit design is a dynamic research area driven by the growing reliance on battery-powered portable computing and wireless communications products. In addition, it has become critical to the continued

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progress of high-performance and reliable microelectronic systems.

## **Low-Power CMOS VLSI Circuit Design by Kaushik Roy**

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University of Tokyo, 4-6-1 Komaba,  
Meguro-ku, Tokyo 153-8505, Japan ...

## **16-2 315MHz Energy-Efficient Injection-Locked OOK ...**

Practical Low Power Digital VLSI Design  
emphasizes the optimization and trade-  
off techniques that involve power  
dissipation, in the hope that the readers  
are better prepared the next time they  
are pre

## **Practical Low Power Digital VLSI**

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## **Design | SpringerLink**

One of the key features that led to the success of complementary metal-oxide semiconductor, or CMOS, technology was its intrinsic low-power consumption. This meant that circuit designers and electronic design automation (EDA) tools could afford to concentrate on maximizing circuit performance and minimizing circuit area.

## **Power optimization (EDA) - Wikipedia**

Low power CMOS VLSI circuit design  
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J.H Lou, Wiley 1999. SoC Design for  
Embedded Systems

## **VLSI Design - Gogul Ilango**

Nowadays, CMOS-SOI is emerging as a promising solution to continue the CMOS scaling allowing low-power, high



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temperature and “system on chip” applications as well as CMOS-SOI-MEMS/NEMS unique sensing systems for IR and THz imagers.

## **Thermal and noise effects in nanometer CMOS-SOI devices ...**

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## **UNIT-II LOW POWER VLSI DESIGN APPROACHES Low power Design ...**

LOW-VOLTAGE HIGH-SPEED VLSI CIRCUITS . As the CMOS technology scales down, traditional analog/RF circuit design methodologies are also evolving by exploiting innovative circuit techniques such as low-voltage and sub-threshold circuits, and all digital implementations.

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## **Sung-Mo Kang: Research**

Design for low power has become nowadays one of the major concerns for complex, very-large-scale-integration (VLSI) circuits. Deep submicron technology, from 130 nm onwards, poses a new set of design problems related to the power

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